In the United States Patent and Trademark Office

In re Application of: William C. Wille et al. ***Filed:*** June 23, 2003

For: METHOD FOR FORMING DAMASCENE STRUCTURE UTILIZING PLANARIZING MATERIAL COUPLED WITH DIFFUSION BARRIER MATERIAL

Serial Number: 10/604,056

Art Unit: 1765 ***Examiner:*** Eric B. Chen

DECLARATION PURSUANT TO 37 C.F.R. 1.131

Hon. Commissioner of Patents and Trademarks
Alexandria, VA 22313-1450

Sir:

We, William C. WILLE, William COTE, Peter E. BIOLSI, John FRITCHE, Allan UPHAM, and Daniel C. EDELSTEIN, hereby declare that:

1. We are the co-inventors of the subject matter described and claimed in the above-identified patent application.

2. Prior to June 28, 2002, we conceived and reduced to practice a method for forming an etched pattern on a semiconductor substrate, the method comprising the steps of: depositing a thin film on the substrate; depositing a layer of planarizing material on the thin film; depositing a layer of barrier material on the layer of planarizing material; depositing at least one layer of imaging material on the layer of barrier material; forming at least one first pattern shape in the layers of imaging material, barrier material and planarizing material; removing the imaging material, either after or concurrently with forming the first pattern shape in the planarizing

material; and transferring the first pattern shape to the thin film. This method optionally further includes the step of forming at least one second pattern shape in the thin film prior to depositing the layer of planarizing material, wherein the second pattern shape is filled with the planarizing material.

3. Prior to June 28, 2002, we also conceived and reduced to practice a method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor, the method comprising the steps of: depositing a dielectric material on the substrate; forming at least one via in the dielectric material, such that at least one of the vias is positioned over the patterned conductor; depositing a layer of planarizing material on the dielectric material and in the via; depositing a layer of barrier material on the layer of planarizing material; depositing at least one layer of imaging material on the layer of barrier material; forming at least one trench in the layers of imaging material, barrier material and planarizing material, such that at least one of the trenches is positioned over the via; removing the imaging material, either after or concurrently with forming the trench in the planarizing material; and transferring the at least one trench to the dielectric material, such that at least one of the trenches is positioned over the via.

4. As evidence of the conception and reduction to practice of the methods referred to in paragraphs 2 and 3 prior to June 28, 2002, attached hereto are two SEM photomicrographs of a semiconductor substrate with a partially etched pattern formed using these methods. The second attached SEM photo is the same as the first attached SEM photo, except that the second SEM photo includes labels identifying various layers and materials.

5. The structure shown in the attached SEM photo was formed as follows. First, a thin film (dielectric) was deposited on the substrate. Next, vias were formed in the thin film, the vias being positioned over patterned conductors in the substrate. (These vias were formed using the method of the present invention.) After forming the vias, a layer of planarizing material (NFC) was deposited on the thin film and in the vias. (NFC is the preferred PHS-based planarizing material described in the

specification of the above-identified application.) Then a layer of barrier material (LTO) was deposited on the layer of planarizing material, and a layer of imaging material (photoresist) was deposited on the layer of barrier material. (The imaging material is not shown because this SEM photo was taken after removal of the imaging material.) Troughs or trenches were then formed in the layers of imaging material, barrier material and planarizing material. Several of the trenches are shown positioned over the vias. The imaging material was removed concurrently with forming the troughs or trenches in the planarizing material. The attached SEM photo was taken just prior to the trough or trench pattern being transferred to the thin film. Other wafers processed in the same lot were subsequently etched to transfer the trough or trench pattern to the thin film.

6. We do hereby declare that all statements made herein of our own knowledge are true, and that all statements made on information and belief are believed to the true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and that such willful false statements may jeopardize the validity or enforceability of the patent.

Respectfully Submitted,

William C Wille 2/22/05		William J Cote 2-22-05	
William C. WILLE	Date	William COTE	Date
Peter E. Biolsi 2/22/05		2-22-05	
Peter E. BIOLSI	Date	John FRITCHE	Date
Allan Upham 2/23/05		Daniel C. Edelstein 2/22/05	
Allan UPHAM	Date	Daniel C. EDELSTEIN	Date

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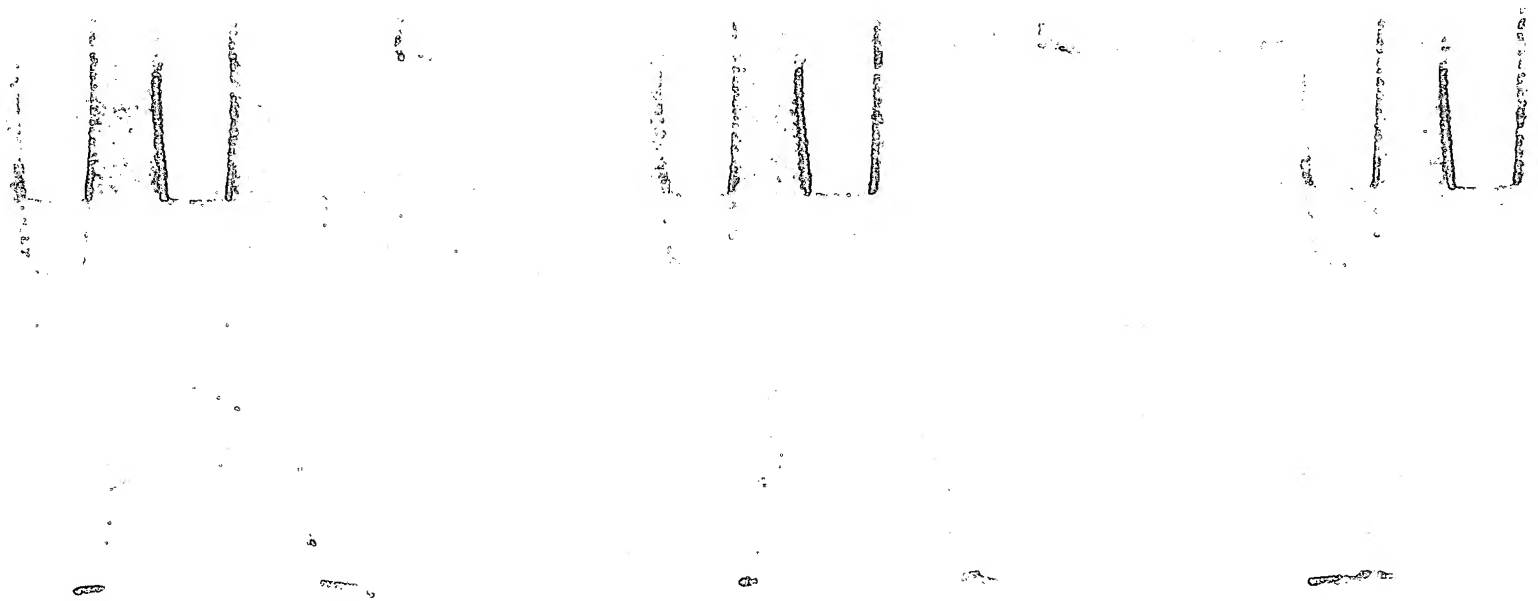

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J.MURPHY

S-5200D 4.0kV -0.2mm x25.0k MIX 4/27/02

1.20um